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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Steven K. Hsu et al.
Title: VOLTAGE-LEVEL CONVERTER

Docket No.: 884.453US1
Filed: June 29, 2001
Examiner: Anh Q. Tran

Serial No.: 09/896,523
Due Date: August 8, 2002
Group Art Unit: 2819

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

A return postcard.
 An Amendment and Response Under 37 CFR 1.111 (3 Pages).
 Clean Version of Pending Claims (2 pgs.).

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 18 day of June, 2002.

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AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.111

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Applicant has reviewed the office action mailed on May 8, 2002. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1 and 2, and addition of new claims 29-32. The specific amendments to individual claims and the new claims are detailed in the following marked up set of claims.

Spec C1

B1

1. (Amended) A voltage-level converter comprising:
~~a static voltage-level converter including an inverter coupled to no more than two transistors in the static voltage-level converter; and~~
~~a split-level output circuit coupled to the static voltage-level converter.~~

2. (Amended) The voltage-level converter of claim 1, wherein the static voltage-level converter comprises:
~~an input node, a first output node, and a second output node;~~
~~a first pair of transistors connected in series, the first pair of transistors including a first transistor and a second transistor, the first transistor coupled to the input node;~~
~~a second pair of transistors connected in series, the second pair of transistors including a first transistor and a second transistor, the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to the first output node[; and], wherein [an] the inverter is coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node.~~

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